Towards Ultra-low Power OFDMA Downlink Demodulation

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ABSTRACT

OFDMA downlink design allowing parallel processing OFDM subcarriers is adopted by a number of commercial wireless standards such as LTE, 5G, and 802.11ax. However, the widespread adoption of OFDMA downlink on low-end IoT devices is stymied due to the existing digital receiver framework's ≈100 mW power consumption, which is mainly incurred by LO+mixer, ADC, and complex digital processing. In this paper, we present an ultra-low-power OFDMA downlink demodulation design, which achieves ≈100 µW receiving power. Our basic idea is to transform the current digital demodulation approach into the analog one based on filtering, which avoids those power-hungry components. We achieve this by proposing a series of novel RF front-end hardware designs: 1) a μW-level two-stage mixing scheme that enables adjustable and precise subcarrier filtering, 2) a quartz crystal-based filter circuit incurring negligible insertion loss, and 3) a passive phase-to-envelope conversion technique enabling low-power non-coherent phase demodulation. We build a prototype to verify the proposed schemes. Experimental and IC simulation results show that: our new design can achieve 130 – 1500 times power savings depending on the number of subcarriers that need to be processed in parallel, compared with the traditional all-digital design.

CCS CONCEPTS

• **Networks** → **End nodes**; • **Hardware**;

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1 INTRODUCTION

Orthogonal frequency division multiple access (OFDMA) based downlink design is embraced by a number of globally influential wireless standards, such as LTE [1–5], 5G [2, 3, 6–9] and 802.11ax [10–13]. The key idea of OFDMA is to create an array of subcarriers that are orthogonal to each other in the frequency domain to transmit data over a range of frequency band in parallel. In practice, subcarriers are further divided into resource blocks (RBs) on the time axis, each of which carries one symbol. Such RBs are designated to different end receivers but organized as a whole into the orthogonal frequency division multiplexing (OFDM) symbol for downlink broadcasting.

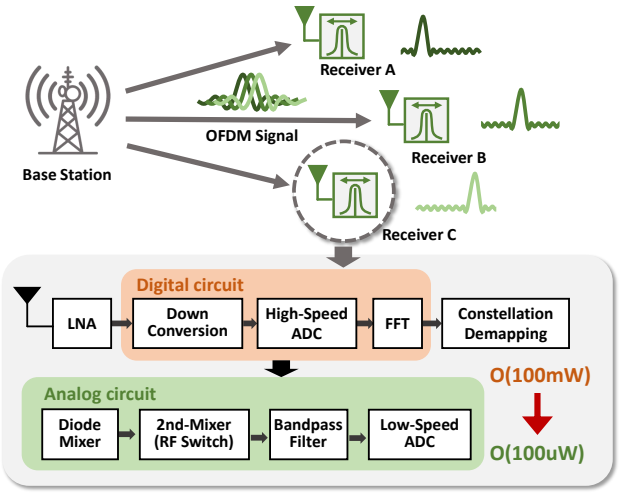

Figure 1: OFDMA downlink.

OFDMA downlink is built on two cornerstone digital signal processing techniques: fast Fourier transform (FFT) and inverse FFT (IFFT). IFFT transforms frequency domain symbols into time domain signals in the downlink transmitter, while FFT does the reverse in the downlink receiver, which retrieves those RBs designated to the local receiver for demodulation, as shown in Fig. 1. The design works smoothly for mobile broadband applications such as high resolution video streaming, where the end terminal is assigned numerous RBs for high data rate. However, the demands of IoT use cases are quite different: the downlink data rate is very low with only single tone or a small number of subcarriers needed, but the battery life expectation is in the level of 10 years. Squeezing the receiver's energy budget thus becomes a must for IoT applications.

The main means for current standardized OFDMA networks to reduce power consumption of the terminal is based on duty cycling. In particular, narrowband Internet of things (NB-IoT) and LTE for machine-type communications (LTE-M) are LTE variants dedicated for IoT applications, which provide power saving mode (PSM), discontinuous reception (DRX) and extended idle model DRX (eDRX) mechanisms for mitigating terminal energy consumption.

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Transceivers negotiate the paging time so that the time for the receiver to monitor the paging channel is shortened. The design philosophy is also adopted by Wi-Fi, which is termed as target waiting time (TWT) in the 11ax context [11, 13–17].

The duty cycling based scheme is an effective engineering compromise, but can hardly touch the essence of low-power demand, because the terminal's power consumption in the wake state is still high. This hinders applications that rely on frequent downlink data reception. For example, electronic price tags vast deployed in the supermarket, where the number displayed on each tag changes over time; smart badges in the intelligent manufacturing scenario, where each worker's badge may receive different instructions from the management system. Even with the sleeping mode, the commercial NB-IoT device's receiving power consumption is still in ≈100 mW [18, 19], and the 11ax device's power consumption is reduced by only 30% [13].

In this paper, we present an ultra-low power OFDMA downlink demodulation scheme, which is able to maintain the terminal's receiving power in ≈100 µW even in the wake state. Our basic idea is to transform the current digital OFDMA downlink demodulation approach into the analog one based on filtering, as shown in lower part of Fig. 1. In particular, we manage to take the desired subcarrier from the entire OFDM symbol for demodulation using ultra-low power analog circuits, which avoids the power-hungry LO+mixer, high-speed ADC and FFT module in the traditional digital receiver framework.

The filtering based design encounters the following new conundrums.

- *The filter's center frequency is unadjustable.* The OFDMA terminals are assigned different subcarriers with different center frequencies, thus the uniformly designed demodulation circuit needs the filter with adjustable center frequency to separate the desired subcarrier. However, the center frequency of the filter as an analog device is fixed.
- *The LC filter's insertion loss is high under narrow bandwidth and high selectivity.* The new design requires a bandpass filter that is able to separate a single subcarrier out from the OFDM symbol, which requires the filter's narrow bandwidth and high selectivity. Bandpass filters commonly used in OFDMA receivers all have LC structures, which means high-order structure thus leading to high insertion loss due to the unavoidable resistance in the inductors.
- *The power consumption of coherent demodulation is high.* The OFDMA transmitter uses phase modulation, thus the receiver normally utilizes coherent demodulation to obtain the information loaded on the subcarrier. However, the coherent demodulation scheme adopted by the regular OFDM demodulator needs high power budget.

In dealing with those challenges mentioned above, we make the following technical contributions:

- We propose a novel two-stage mixing scheme that enables adjustable subcarrier separation using filters with fixed passband. The key is to adjust frequency of the received OFDM symbol in a coarse-to-fine manner. Specifically, we first down-convert the received OFDM symbol to a fixed intermediate frequency (IF) band, and then take out the target subcarrier with a fine-grained mixing. In particular, for the target subcarrier #n with bandwidth ΔBW, we mix the IF signal with a square wave in frequency $n \times \Delta BW$ to move the target subcarrier to the filter's passband. The entire mixing operation costs μW-level power.
- We find that the quartz crystal filter can resolve the high insertion loss issue. The LC filter incurs high insertion loss mainly due to the thermal effect, which always occurs when the current passes through the LC filter's inner resistor. However, the quartz crystal resonates based on the piezoelectric effect; the electrical power can be directly converted to mechanical power thus incurs negligible insertion loss.
- We reveal an interesting phenomenon: the BPSK signal decreases in envelope amplitude at each 0-to-π phase flip point when passing through the narrow bandpass filter. Based on the phenomenon, we propose a passive phase-to-envelope conversion scheme that enables the non-coherent phase demodulation. This further reduces the demodulation power consumption.
- We build a hardware prototype to verify our design, based on which we conduct experiments and IC simulations to evaluate the prototype system's performance. Results show that our new design can achieve 130 − 1500× power saving depending on the number of subcarriers need to be processed in parallel, compared with the traditional all-digital design.

Platform availability. Our OFDMA downlink receiver hardware, including schematics and layout, as well as the software for SDR control and the detailed performance data of the analog front-end will be released for academic use, and available online [20].

2 PRELIMINARIES

2.1 OFDMA Digital Downlink

In the OFDMA downlink architecture, the base station or the access point serves as TX and the terminal as the RX. OFDMA TX transmits the bit stream in parallel. For example, the TX delivers symbols '00', '01', '10' and '11' in parallel with different subcarriers. This is known as the orthogonal frequency division multiplexing (OFDM) modulation scheme. Theoretically, each subcarrier could be generated by an independent local oscillator to form a separate transmission hardware chain block, and the same number of oscillators are also needed at the RX for demodulation. However, the corresponding hardware complexities and very high power consumption make such straightforward implementation unrealistic.

The practical OFDMA TX leverages digital signal processing techniques. Instead of using a large number of oscillators, the IFFT module is used to convert those parallel frequency domain signals into samples of a composite time domain signals. That is, IFFT could compute the same sampled signal as would have been generated by those parallel oscillator transmission chains after sampling. Thus the TX only needs to feed results of IFFT into the digital-to-analog converter (DAC), and then performs up conversion to transmit the time domain signal. The RX basically does the reverse when receiving the signal. After down conversion and ADC, the sampled signal goes through the FFT module to output demodulated symbols in parallel.

2.2 Optimization for Power Saving

The digital OFDMA downlink design based on IFFT and FFT can process multiple subcarriers effectively, but the digital signal processing modules as well as corresponding DAC and ADC are power hungry. This might be insignificant for a TX with wired power

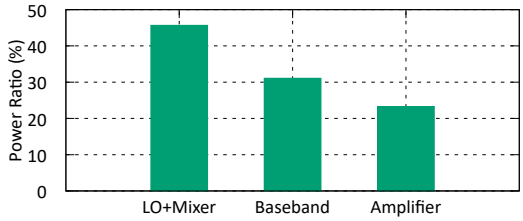


Figure 2: NB-IoT receiver's power consumption.

supply, but could significantly affect the battery life expectation of the RX. In order to accommodate IoT applications with very limited energy budgets, simplifications are applied to the OFDMA downlink, where the major methods are to reduce the number of subcarriers and increase the sleeping time of the terminal. The representative example is the NB-IoT system, which reuses the LTE OFDMA digital downlink architecture with following optimizations for power saving.

The NB-IoT downlink occupies only 12 subcarriers, which corresponds to one physical resource block (PRB) with 180 kHz [8, 19, 21–26]. The modulation techniques are limited to only QPSK or BPSK, and the transport block sizes (TBS) can be smaller than a single PRB [8, 21, 23–26]. The duty cycling based schemes make the NB-IoT transceiver inactive most of the time. DRX scheme regulates the time spent in active listening and time interval between the beginning of two active listening [27–30]. eDRX mechanism specifies the duration of paging termed as paging time window (PTW) and time interval of two PTWs [8, 25, 31–33]. PSM scheme regulates the duration of listening for paging, as well as the interval between two tracking area updates (for updating location information) [10, 31, 32, 34–36].

Moreover, the NB-IoT abandons some functionalities of LTE to decrease the signaling overhead, including inter radio access technology (RAT) mobility, handover mechanisms, public warning, dual connectivity, carrier aggregation and emergency calling [8, 21, 23–26]. New transmission procedures based on cellular IoT evolved packet system (CIoT EPS) are developed especially supporting small bursts of data. The user plane of EPS ensures terminals to cache radio resource control (RRC) protocol information when entering into an inactive state, saving the energy for establishing a new RRC connection upon waking-up.

2.3 Power Consumption Analysis

While the NB-IoT provides a series of optimizations to the OFDMA digital downlink in a systematical manner and realize overall power saving, the receiving power consumption of the commercial NB-IoT terminal is still in ≈100 mW [18, 19]. Some academic efforts have been dedicated to further optimize the duty-cycling based mechanisms with prediction algorithms [37–39], but turn out yielding only 5 – 34% power saving compared with the standardized NB-IoT schemes according to simulation results [40]. The fundamental reason is that the duty-cycling methodology and corresponding system simplification still leave the local oscillator (LO), FFT and ADC in the downlink demodulation procedure untouched, which account for majority of the power consumption.

Since the NB-IoT receiver's IC design is proprietary, we here quantitatively analyze the power consumption composition with a publicly available NB-IoT analog front-end (AFE) IC design presented in [21]. The design contains partial amplification, IQ phase correction and ADC in the (analog) baseband, but does not include digital designs. We complement the digital baseband (mainly the FFT) using Verilog and conduct simulation on the power consumption based on Synopsys DC with SMIC 40nm 1.1V IC process. Figure 2 shows the simulation results. We can see that 78% of total power is from the LO, mixer and baseband. If these components can be replaced by passive components like diodes and RLC, then the power consumption can be significantly reduced. Next, we will show that the power consumption of the power amplifier can also be significantly reduced. We note that the power consumption of an amplifier is positively related to both the amplification gain and the bandwidth of the input signal:

$$P_{Amp} \propto G \cdot P_{in} = G \cdot BW \cdot \mathrm{PSD}_{in}, \tag{1}$$

where G is the amplification gain, P_{in} is the power of the input signal, BW is the input signal bandwidth, and PSD_{in} is the power spectrum density (PSD) of the input signal. Here we assume that the signal has a uniform PSD over its bandwidth, which is true for existing OFDM systems including NB-IoT and Wi-Fi because all subcarriers use a consistent constellation diagram in modulation. Classic OFDMA receiver has to amplify the whole bandwidth of the raw OFDM signal due to its digital architecture: subcarrier separation happens in the digital domain (by using FFT) after the amplifier and the ADC. However, for a specific OFDMA receiver, its own payload only lies in a small portion of subcarriers. If a user only occupies 10% bandwidth, then the power consumption of the amplifier can be reduced by 90% with perfect filtering before amplification. Based on the above analysis, we can find that most of the power of existing NB-IoT OFDMA receiver can be optimized or potentially reduced: $R = 46\% + 31\% + 90\% \times 24\% = 98.6\%$. This ratio can be even higher if we sacrifice some sensitivity and further reduce the productive bandwidth of the receiver. The room for power optimization for an OFDMA receiver hardware design is huge.

3 SYSTEM OVERVIEW

We present a novel receiver architecture under the low-data rate scenario that each user is allocated with one or very few subcarriers in the OFDMA system. Such hardware architecture reduces the power consumption of an OFDMA receiver to $100\mu W$-level by extracting and demodulating the subcarrier using an analog framework. This can significantly prolong the operating time for IoT devices without the expense of wake time.

3.1 Basic Idea and Challenges

Figure 3 sketches out the idea of our ultra-low-power analog OFDMA demodulation approach. We achieve this ultra-low-power design with the following two innovations:

- Different from the traditional OFDMA demodulation where the receiver needs to perform all the front-end operations (A/D conversion, amplification, and FFT) on the whole bandwidth, we propose to first extract the target subcarrier. Then the subsequent operations can be performed on a narrow band, which substantially reduces the energy consumption.
- We propose a low-power PSK demodulator, which can use envelope detection to demodulate the PSK subcarrier signal, instead of using the energy consuming coherent detection.

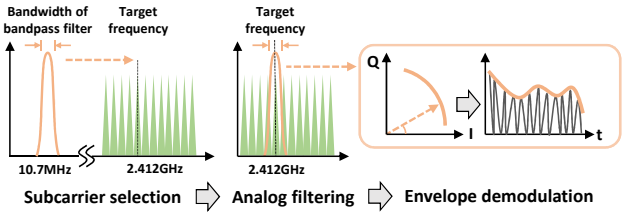


Figure 3: Basic idea of this work. The ultra-low power demodulator circuit first selects the assigned subcarrier, then it applies analog filtering to filter out the subcarrier and finally performs envelope demodulation to obtain bits.

The following issues have to be addressed before we could carry out the new framework.

C1: Precise filter frequency adjustment. To take one specific subcarrier from the OFDM symbol containing multiple subcarriers, we need to first precisely align the filter frequency with the target subcarrier. However, most filters used in today's RF front-end only have fixed frequency. Although variable capacitors can realize programmable filter by continuously changing the center frequency of the LC filter, it still encounters the issue of bandwidth expansion under different frequency settings. For example, if we use a third-order Chebyshev LC filter as illustrated in Fig. 4(a), the magnitude response of the filter encounters a 41% bandwidth expansion when we reduce the capacitance to increase its frequency from 10.7 MHz to 11.2 MHz, as shown in Fig. 4(b).

C2: Narrow bandpass filtering. To separate the target subcarrier from the OFDM symbol, we also need an executing analog filter which simultaneously achieves narrow passband and low insertion loss. However, no existing filter satisfies both of the two requirements. To realize narrow bandpass filtering, a filter with a high-order (LC) structure is a usual choice as recommended in NB-IoT standard [41]. Such design however will inevitably introduce high insertion loss due to inner resistance of the inductor. Specifically, the inductor can be modelled as an ideal resistor connected with an ideal inductor. Even with tiny value in O(0.001Ω), the resistor indeed incurs considerable insertion loss. In Fig. 4(c), we simulate a Chebyshev third-order LC filter with the center frequency of 10.7 MHz in Advanced Design Systems (ADS). The resistor in each inductor is set to be 0.001Ω. As can be seen, the filter insertion loss reaches around 30 dB. The value will continue to rise if the filter's order increases further.

C3: Phase to envelope conversion. To carry out PSK demodulation with low-power envelope detection, a critical step is to realize low-power phase-to-envelope conversion, which is still a open issue to the best of our knowledge. Recently proposed low-power receiver designs [42–44] only realize frequency-to-envelope conversion, leveraging the transition region of the filter. However, subcarrier frequency is fixed in PSK modulation, thus those existing designs hardly can be borrowed to address the issue.

3.2 Key Designs

We here first provide a high-level description of key designs to deal with challenges mentioned above, which is illustrated in Fig. 5. Details are to be provided in Section 4.

Subcarrier separation. As it is difficult to directly modify the the filter's center frequency, we instead adjust the frequency

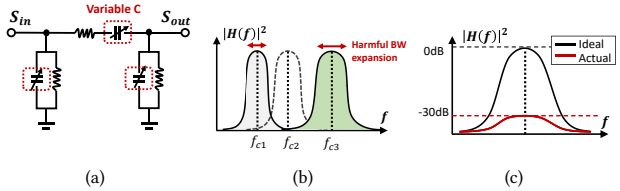


Figure 4: (a) Structure of a third-order Chebyshev LC filter. (b) Bandwidth expansion. (c) High insertion loss.

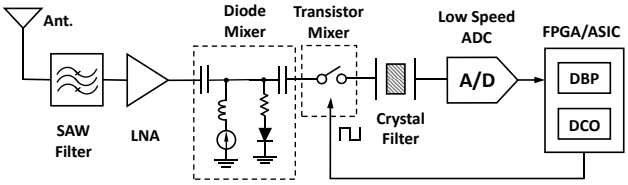


Figure 5: Receiver circuit design.

of the received OFDM symbol to the filter's passband. The pure LO+Mixer structure can realize fine-grained frequency control in down-conversion yet consumes high power when performing on RF-band signal, as shown in Fig. 2; diode passive down-conversion consumes ultra-low power but cannot be adjustable [42, 45]. We integrate the two filtering schemes to propose a coarse-to-fine design. As shown in Fig. 5, we first use a diode passive down-conversion mixer to coarsely convert the input signal from RF band to IF band. We then use an IF mixer driven by an adjustable low frequency ($0 \sim 120$ kHz) digital controlled oscillator (DCO) to move the signal to the target frequency precisely. The two-stages mixing solution finally achieves adjustable subcarrier filtering with μW-level power consumption. We note that the second mixer is low-power because the IC dynamic power follows the rule $P_{Dynamic} \propto f$. Compared to the GHz-level LO used in classic receivers, our DCO only generates 120 kHz signal in the worst case, which results in 10^4 more power savings in the down-conversion step. This issue will be elaborated in Section 4.1.

Analog filtering. We propose to use a quartz crystal filter as shown in Fig. 5 to perform the task of taking out the target subcarrier from the OFDM symbol. The quartz crystal can realize extremely narrow bandwidth with ultra-low insertion loss even under the high-order structure. Unlike the inductor that dissipates thermal power when the current passes through the inner resistor, the quartz crystal works based on the piezoelectric effect, which can directly converts electrical power to mechanical power. The crystal filter introduces almost no thermal effect, thus incurs negligible insertion loss. Our experiments show that a crystal filter can successfully separate out one subcarrier with less than 1.5 dB insertion loss.

Envelope demodulation. We achieve phase to envelope conversion based on the observation that the PSK modulated signal decreases in envelope amplitude at both the start and the end of a symbol, after passing through a bandpass filter. Such effect becomes especially obvious on the BPSK modulated signal. We will further explain this phenomenon in Section 5. Leveraging this effect, we only need to detect the envelope amplitude decline points, which

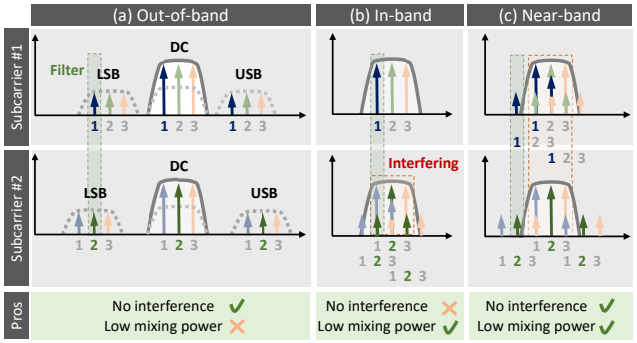


Figure 6: Illustration of second mixing. The dash line denotes the three OFDM signals caused by the two-stage mixing process (see Equ. 7); and each arrow represents a subcarrier inside the OFDM signal.

correspond to BPSK phase flip points, and then perform differential decoding to recover the transmitted data without knowing the original phase. The above process incurs only μW-level power consumption.

4 DETAILED DESIGNS

4.1 Subcarrier Separation

Imagine that the received OFDM symbol at the receiver is like the situation as depicted in Fig. 3. Our purpose is to separate one subcarrier from the OFDM symbol comprised of multiple subcarriers. To this end, the first step is to down-convert the entire OFDM symbol to the IF band, which is realized by a passive Schottky diode as a two-port mixer. Such mixer design consumes very low power as mentioned in [42, 45], which however can provide only a fixed frequency shift. This means that the receiver must be equipped with an LO adjusting the amount of frequency shift, which is infeasible due to the LO's high power. In our design, we let the transmitter send a company signal with the entire OFDM symbol, which is a pure carrier signal with the center frequency Δf away from that of the OFDM symbol. This company carrier signal fulfills the task that would have been accomplished by the LO, while consuming near-zero power at the receiver. The detailed transmitter design is to be presented in Section 4.4.

After the first-stage mixing, the receiver down-converts the RF signal to the IF. The next step is to perform the second-stage mixing, which is to further shift the IF signal in finer granularity. This is realized by a transistor switch driven by a digital controller oscillator (DCO) as shown in Fig. 5. The DCO can be reprogrammed by the baseband command according to frequency of the target subcarrier. In the second-stage mixing, we can regard the switch's on/off as the 1/0 signal switching, then the switching signal can be expressed as:

$$f(t) = \sum_{n=-\infty}^{\infty} \varepsilon\left(t + \frac{\tau}{2} + nT\right) . - \varepsilon\left(t - \frac{\tau}{2} + nT\right), \tag{2}$$

where $\varepsilon(x)$ is a step function that satisfies:

$$\varepsilon(x) = \begin{cases} 1 & \text{for} \quad x \geq 0 \\ 0 & \text{for} \quad x < 0 \end{cases} . \tag{3}$$

We can see that T is the on-off period of the switch, τ represents the duration of state 'on' in each on-off period. The expression above in the form of a Fourier series is:

$$f(t) = \frac{\tau}{T} + \frac{\tau\omega_0}{\pi} \sum_{n=1}^{\infty} Sa\left(\frac{n\omega_0\tau}{2}\right) cos\left(n\omega_0 t\right), \tag{4}$$

where $Sa(x)$ is the unnormalized sinc function that satisfies

$$Sa(x) = \frac{sinx}{x} \tag{5}$$

and ω_0 is the angular frequency corresponding to the switching period T: $\omega_0 = 2\pi/T$. Now we let $n = 2k + 1$ and $\tau = T/2$, then:

$$f(t) = \frac{1}{2} + \frac{2}{\pi} \sum_{k=0}^{\infty} \frac{1}{(2k+1)} sin\left(\frac{(2k+1)\,\pi}{2}\right) cos\left((2k+1)\,\omega_0 t\right). \tag{6}$$

We ignore terms representing third or higher order harmonics because those components are negligible in amplitude. We reserve the term when $k = 0$, and the switch signal becomes:

$$f(t) \approx \frac{1}{2} + \frac{1}{\pi} e^{-j\omega_0 t} + \frac{1}{\pi} e^{j\omega_0 t}. \tag{7}$$

Analyzing the expression of $f(t)$, we can find that the spectrum of the IF signal after the second-stage mixing is as shown in Fig. 6, which mainly consists of 3 frequency components. The term $\frac{1}{2}$ indicates the DC component of the original IF signal, and the rest two with coefficient $\frac{1}{\pi}$ are lower sideband (LSB) shifted signal and upper sideband (USB) shifted signal, respectively. The amount of frequency shift is determined by ω, which can be controlled by the square wave generation process.

In choosing the center frequency of the filter, we need to strike a balance between power efficiency and interference. Specifically, to avoid interference, a large amount of frequency shift is required, which however introduces high energy consumption to produce a high-frequency square wave signal that drives the transistor mixer. For example, Fig. 6(a) shows the case of out-of-band filtering. To produce the LSB and the USB that have no overlap with the DC band, the receiver has to produce a square wave signal with a frequency that is larger than the bandwidth of the OFDM signal (e.g., $\omega/2\pi \geq BW$). This is obviously inefficient in power consumption. To solve this problem, an alternative is to perform in-band filtering, where the receiver introduces only a small amount of frequency shift and thus the LSB and USB are partially overlapped with the DC band as shown in Fig. 6(b). Though this method can largely reduce the power consumption since the receiver only has to produce a low frequency square wave signal (i.e., $\omega = 0$), it suffers from serious interference from both DC and USB.

We overcome the above dilemma by performing near-band filtering. In particular, we set the filter pass band close to the the left side of the OFDM signal as shown in Fig. 6(c). Then the receiver only has to produce a square wave signal with the frequency of $n \times \Delta BW$ to separate an arbitrary subcarrier n. The maximum mixing frequency produced by the DCO is no greater than BW. As we will show, the final BW is around 120 kHz. We will show that this low DCO frequency is extremely beneficial in the following two questions: (1) why the DCO and second mixing can be low power? (2) Why CFO is not a critical issue?

Why the DCO and second mixing can be low power? To answer this question, we first analyze the power components of an IC circuit. Its power consumption consists of two parts: static power and dynamic power. The static power is consumed by the leakage current in MOSFETs while the dynamic power is consumed during MOSFETs' being turned on and off. In our circuit, dynamic power is the dominant factor because the static power of an oscillator is typically within ≈100 nW and negligible when built with 40nm IC process. The dynamic power can be estimated with [46]:

$$P_{Dynamic} = \sum_{i=1} V_{CC}^2 \times f_i \times C_i \times N_i \tag{8}$$

where V_{CC} is the supply voltage of the transistors, f_i is the switching frequency of the i^{th} transistor, C_i is the load capacitor of the output switching signal, and N_i is the number of the transistors that switch at frequency f_i. We can find that when the circuit structures (same N_i) and the parameters (the same supply voltage V_{CC} and the same capacitance (C)) are the same, the dynamic power is proportional to the switching frequency f. The LO and mixer in normal GSM receiver circuit consumes *O(10mW)* under 1-2 GHz rate. Reducing the operation frequency to the scale of 100 kHz can bring 10^4 more power reduction, which is around 1 µW.

Why CFO is not a critical issue? we first analyze why CFO is a critical issue in normal receivers; then we show that in our design, the CFO is negligible. A classic receiver uses an LO to generate the exact frequency of the carrier f_s. Typically, the oscillator's frequency variation (usually termed as *stability* in datasheets) in a communication circuit is around 10 ppm. So the CFO can be calculated as $\Delta f = f_s \times 10/10^6$. For a receiver that works at the 1 GHz band, the actual oscillation frequency can be $f_{RX} = 1\,\text{GHz} \pm 10\,\text{kHz}$. Similarly, the frequency of the transmitter can be $f_{TX} = 1\,\text{GHz} \pm 10\,\text{kHz}$. Since f_{TX} and f_{RX} are generated by different oscillators, they are independent. The measured CFO at the receiver side is $f_{CFO} = f_{TX} - f_{RX}$, which can be 20 kHz in the worst case. Such a frequency error would cause serious issues in the demodulation process, therefore CFO must be corrected in a normal receiver. However, in our two-stage mixing process, our receiver does not generate the full LO. Instead, the LO is provided by the transmitter in the first passive mixing stage. Thus, the common-mode CFO is removed by the diode:

$$f_{CFO} = (f_C + \Delta f_{TX}) - (f_C + \Delta f_{TX}) = 0 \tag{9}$$

where f_C is the carrier frequency. Then the frequency error is caused by two factors: the SFO of the transmitter and the DCO frequency error at the receiver. Their maximum frequency error can be estimated as follows:

$$f_{Err} = f_{IF} \times 10/10^6 + f_{DCO} \times 10/10^6 \tag{10}$$

where f_{IF} is the IF frequency (10.7 MHz), and f_{DCO} is around 120 kHz. Finally, f_{Err} can be calculated to be around 0.1 kHz, which is not a critical issue for demodulation. This frequency error is also emulated in our evaluations in Section 6.1; and the results show that the ±0.4 kHz is the safety margin. The maximum possible frequency error of our circuit obviously lies within this range.

4.2 Analog Filtering

After the two-stage mixing procedure described above, the IF signal is ready for filtering. We now present detailed design of the crystal filter circuit. As mentioned in Section 3.1, we need a low power filter that is steep at both ends, so that the target subcarrier can be completely separated without distortion. In particular, we need both ends of the filter perfectly lie on the center frequencies of the target subcarrier's neighboring subcarriers, in order to eliminate the interference.

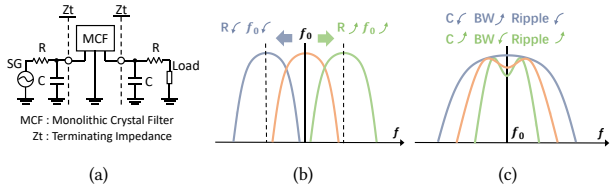


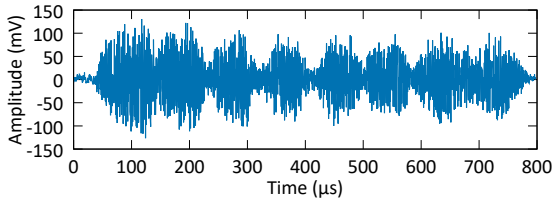
Figure 7: Crystal filter design. (a) Circuit structure of a 2-pole crystal filter. (b) R impacts filter central frequency. (c) C impacts filter ripples.

To what extent the filter is sharp at both ends can be measured by the filter's selectivity $S = \frac{f_c}{f_\infty - f_c}$ [47], where f_c is the cut-off frequency and f_∞ is the frequency of the nearest subcarrier's pole outside the passband. In our design, the OFDMA symbol's center frequency is set to be 10.7 MHz, the subcarrier spacing 1010 kHz, and the expected filter cutoff frequency about 4 kHz, then $S = \frac{f_c}{BW-(f_c-f_0)} \approx 1000$. Such selectivity is extremely high, which only can possibly be achieved with crystal-based filters.

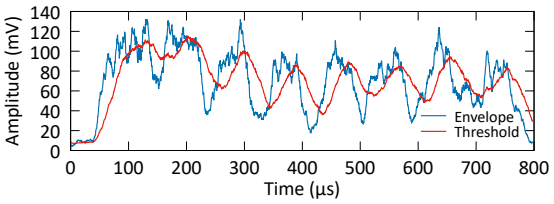
To connect the crystal filter to the circuit, we must pay special attention to the impedance matching process. The impedance matching circuit is normally in the LC form, consisting of an inductor and a capacitor. However, the crystal filter impedance matching circuit is as shown in Fig. 7. We regard SG as the signal source, which actually is the part of the circuit before the crystal filter circuit. The resistance of the circuit after can be regarded as a resistor load. The goal of the impedance matching is to adjust the values of R and C, so that the resistance of the crystal filter circuit and the resistance load after equal to the internal resistance of the SG.

However, the impedance matching procedure will also impact the properties of the crystal filter. In particular, we need to perform impedance component (R) matching, capacitance component (C) matching, and inter-stage capacity (Cc) matching. In our design, we need to determine R and C values for a raw monolithic crystal filter (MCF). As shown in Fig. 7, R component determines center frequency of the filter. Increasing and decreasing value of R will increase and decrease the center frequency of the filter, respectively. The C component determines the ripple size and passband bandwidth. When the capacitance value becomes smaller, the waveform width becomes wider, the passband width and attenuation band width become wider, meanwhile the top distortion disappears and the ripple size decreases.

Note that C matching is challenging in our circuits. The capacitor required is usually with a value of a few pFs, which is even less than the coupling capacitance between the pads on the PCB thus making the matching impossible. To address this issue, we put inductors in parallel with the pads before these tiny pF-level capacitors are soldered. The function of the inductor is to coarsely eliminate the coupling capacitance. Moreover, C matching can be



(a) Phase-to-envelope conversion of a subcarrier.



(b) BPSK demodulation in the DBP.

Figure 8: Envelope conversion and demodulation.

even harder for crystal filters with four or more poles although their selectivity performance is better than that of the two-pole filters. The crux is the inter-stage capacitance, which can cause severe nonlinear effects in the filter passband if not perfectly matched. The phenomenon is that the filter has a strong ripple either on the lower-frequency side of the passband or on the higher-frequency side of the passband. We finally choose to use two-pole crystal filters in our design because the two-pole filter has already achieved enough selectivity.

4.3 Envelope Demodulation

The separated subcarrier has actually been loaded with information by PSK modulation at the transmitter, which needs demodulation so that the receiver can retrieve the information conveyed. The OFDMA receiver normally utilizes coherent detection for demodulating, which however consumes much power. We here first reveal that the constant-envelope PSK signal would experience envelope changes after going through a bandpass filter with the same center frequency and similar bandwidth. Leveraging such phenomenon, we could translate the modulated signal's phase change into the amplitude change. The translated signal ideally could be demodulated using the passive envelope detection circuit, which however could restrain the receiving data rate. We then introduce a ultra-low power ADC with low sampling rate to realize demodulation.

■ **Phase-to-envelope conversion.** Figure 8(a) shows the phenomenon of phase-to-envelope conversion, which is an example of BPSK signal. The data payload in the example is '1010...10', we can see that the envelope becomes an OOK signal with '10' alternating. This is because when a symbol is π phase difference from the successor, the envelope would decrease to approximately zero at the phase flip point.

The fundamental reason of the phenomenon is the effect of the bandpass filter. Suppose that the baseband signal at the transmitter after BPSK constellation mapping is:

$$b(t) = \sum_{n=0}^{\infty} a_n g(t - nT), \tag{11}$$

where a_n represents the possible payloads ± 1, and we assume that the two values appear in equal probability. After modulation, the signal becomes:

$$x(t) = \left[\sum_{n=0}^{\infty} a_n g(t - nT)\right] \cdot e^{j\omega_0 t}, \tag{12}$$

where $\omega_0/2\pi$ is the carrier frequency and $\omega_0 \gg \frac{2\pi}{T}$. The bandpass filter with bandwidth $\frac{1}{T}$ and center frequency ω_0 has the time domain response:

$$h(t) = \frac{sin\left(\frac{\pi t}{T}\right)}{\pi t} \cdot e^{j\omega_0 t}. \tag{13}$$

Then the BPSK signal after going through the filter becomes:

$$\begin{aligned} y(t) &= x(t) * h(t) \\ &= \int_{-\infty}^{\infty} x(\tau)\, h(t-\tau)\, d\tau = \int_{-\infty}^{\infty} x(t-\tau)\, h(\tau)\, d \\ &= \int_{-\infty}^{\infty} \frac{sin\left(\frac{\pi\tau}{T}\right)}{\pi\tau} e^{j\omega_0\tau} \left[\sum_{n=0}^{\infty} a_n g(t-\tau-nT)\right] e^{j\omega_0(t-\tau)} d\tau \\ &= e^{j\omega_0 t} \int_{-\infty}^{\infty} \frac{sin\left(\frac{\pi\tau}{T}\right)}{\pi\tau} \left[\sum_{n=0}^{\infty} a_n g(t-\tau-nT)\right] d\tau. \end{aligned} \tag{14}$$

For simplicity, we let $x_1(t) = \sum_{n=0}^{\infty} a_n g(t - nT)$, and that $h_1(t) = sin(\pi t/T)/(\pi t)$, $y_1(t) = x_1(t) * y_1(t)$, then the signal is in the following form:

$$y(t) = e^{j\omega_0 t}\left[x_1(t) * h_1(t)\right] = e^{j\omega_0 t} \cdot y_1(t). \tag{15}$$

Since $\omega_0 \gg \frac{2\pi}{T}$, $y(t)$ can be regarded as the product of the carrier $e^{j\omega_0 t}$ and the envelope $y_1(t)$, where

$$\begin{aligned} y_1(t) &= \int_{-\infty}^{\infty} h_1(\tau)\, x_1(t-\tau)\, d\tau \\ &= \int_{-\infty}^{\infty} \frac{sin\left(\frac{\pi\tau}{T}\right)}{\pi\tau} \cdot \sum_{n=0}^{\infty} a_n g(t-\tau-nT) d\tau. \end{aligned} \tag{16}$$

When $t = KT$, it corresponds to the optimum sampling time at the main lobe. We can obtain:

$$y_1(KT) \approx \int_{-T}^{0} \frac{sin\left(\frac{\pi\tau}{T}\right)}{\pi\tau} \cdot a_k d\tau + \int_{0}^{T} \frac{sin\left(\frac{\pi\tau}{T}\right)}{\pi\tau} \cdot a_{k+1} d\tau. \tag{17}$$

If $a_{k+1} = a_k$, then $y_1(KT) \approx 2\int_0^T \frac{sin(\pi\tau/T)}{\pi\tau} \cdot a_k d\tau$; if $a_{k+1} \neq a_k$, $y_1(KT) \approx 0$. From Eq. (17), we can see that when the data value is ± 1 alternately, the signal mutation point reaches the extreme value of the output amplitude change after filtering.

We could apply Manchester encoding method to avoid the uneven distribution of ± 1 in the data stream, which translates bit '1' to '01' and '0' to '10' to intentionally create '10' sequence. The source coding could reduce the symbol rate but acceptable considering the low data rate requirement of IoT applications.

■ **Digital detection of the envelope.** Ideally, we can use a passive envelope detection circuit with a comparator to convert analog envelope signal to binary digital bits. Such circuits consumes extremely low power and is widely adopted in downlink design of wireless backscatter systems [48–50]. In particular, the envelope data is simultaneously fed into two paths. One path connects to the positive port of the comparator, and the other to an RC integral circuit to produce dynamic thresholds of the comparator. The output of RC circuit connects to the negative port of the comparator.

However, the traditional low-power design can hardly work in our receiver circuit in an effective manner. In particular, we find

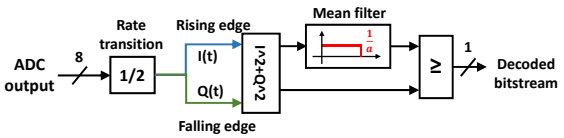


Figure 9: Digital detection logic of the envelope.

in experiments that the high output resistance of the crystal filter limits the choice of the resistor in the RC circuit. That is, we need a high-value R to ensure the threshold circuit's share of power, which however limits the data rate that can be conveyed in the envelope. This is because higher-value R will result in longer charge and discharge time of the RC circuit.

To address the issue, we move the envelope demodulation to the digital baseband processing (DBP) module by using a low power ADC with low sampling rates. We note that the raw signal output from the filter is in the form of $s(t) = a(t)cos(2\pi\Delta f t)$, with Δf is the IF frequency 10.7 MHz and $a(t)$ is the envelope signal. The bandwidth of $a(t)$ can be roughly estimated by the subcarrier data rate 10 kHz. Typically, we are supposed to use an ADC with a sampling frequency larger than $2 \times \Delta f = 21.4$ MHz to satisfy the Nyquist's sampling rate for perfect reconstruction, which requires high power consumption thus neutralizes the benefit of envelope demodulation.

In fact, we could leverage the spectrum aliasing effect of digital sampling. In particular, we could use a sampling clock f_s to sample the I and Q component of $s(t)$. The final envelope is estimated as $I(t)^2 + Q(t)^2$ as shown in Figure 9. In this way, we find that our sampling frequency can be reduced to $m \times 10$ kHz where m is a positive integer which means the oversampling factor. The sampling frequency is prevented to be a non-integer multiple of 10 kHz because a rational resampling filter will be required before bit-level decoding in this case. Then this structure brings extra power consumption. The lowest feasible f_s is 10 kHz but its performance is constrained as will be discussed in Section 6.3. Finally we use 20 kHz sampling frequency. Figure 8(b) depicts how subcarrier signal output from the filter is demodulated with our method. Both the envelope signal and the dynamic threshold signal are obtained by undersampling. We can see that we can still successfully realize envelope demodulation below the Nyquist's rate.

4.4 Transmitter Design

The ultra-low power demodulation as described above requires cooperation of the transmitter. Figure 10 shows a standard OFDM transmitter's baseband workflow, where we need to make the following modifications:

■ **Modulation.** We modify the modulation to DBPSK. As explained in Section 4.3, the receiver detects the envelope decline and performs differential decoding. Thus the transmitter also needs to apply differential BPSK for matching.

■ **Serial to parallel (S/P) conversion.** The S/P conversion module needs to interleave each receiver's data to the corresponding subcarrier. Besides, the transmitter needs to assign the company pure-tone signal and the OFDM subcarriers to appropriate FFT bins. We set the IFFT size to be 4096 under $fs = 40$ MHz DAC sampling rate. Then the subcarrier spacing is 9.8 kHz. The company signal is assigned at IFFT bin −584 (−5.7 MHz); and OFDM subcarriers

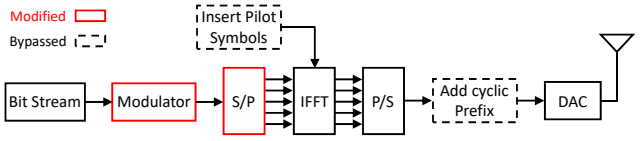


Figure 10: Transmitter design.

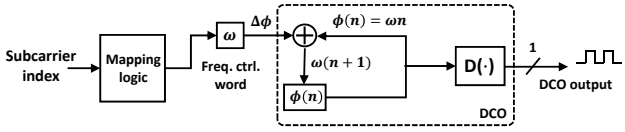


Figure 11: DCO design of DBP. Here $D(\cdot)$ is a decision logic converts the inner phase value to 1-bit wide clock signal.

are assigned at IFFT bins 513 ∼ 524 (5.01 MHz-5.11 MHz). Other subcarriers are filled with zeros.

■ **Bypassing pilot insertion.** Pilots are used to recover phase for coherent detection, which is obviously unnecessary in our design since phase change will be converted to envelope change in the receiver. To elaborate on this issue, we note that the phase continuity/discontinuity between symbols remains unchanged under any phase offset. It means the envelope output will remain the same shape under the phase offset, still leading to successful differential decoding. Therefore, the missing pilot tones used to recover phase offsets are no longer necessary.

■ **Bypassing cyclic prefix (CP) insertion.** Note that the envelope declination phenomenon is maximized when two consecutive symbols experience a $0 - \pi$ phase inversion point. Such $0 - \pi$ phase inversion can be ensured by the single carrier BPSK. In the OFDM+BPSK system, the CP insertion however breaks the $0 - \pi$ inversion. After the IFFT module, the time domain signal becomes

$$x[n] = \frac{1}{N} \sum_{k=0}^{N-1} X[k]\, e^{j\frac{2\pi}{N}kn}, \tag{18}$$

where $x[n]$ represents n^{th} time domain sample and $X[k]$ represents k^{th} frequency domain symbol, and $X[k] \in \{e^{j0}, e^{j\pi}\}$ in DBPSK. Both n and k are in $\{0, 1, ..., N-1\}$ with N the FFT size. We select a subcarrier with index k_0. Suppose CP has a length of M samples, then the starting sample of k_0^{th} subcarrier after CP insertion becomes the $(N-M)^{th}$ sample without CP. This indicates Δp phase offset:

$$\Delta p = angle\left(e^{j\frac{2\pi}{N}k_0(N-M)}\right) = -\frac{2\pi}{N}k_0 M. \tag{19}$$

Such phase offset would reduce the phase flip and degrade the performance.

Note that CP in the traditional OFDM receiver is for preventing ISI during FFT windowing; however, our receiver only demodulates one subcarrier, where there is no such ISI issue. Thus removing CP has no impact on the receiver.

5 IMPLEMENTATIONS

We build a prototype system as shown in Fig. 12 following the designs described above. The system contains customized receivers and the transmitter implemented with WARP v3.

For the receiver, the implementation is based on the design as shown in Fig. 5. We place a TA2238A SAW filter after the antenna

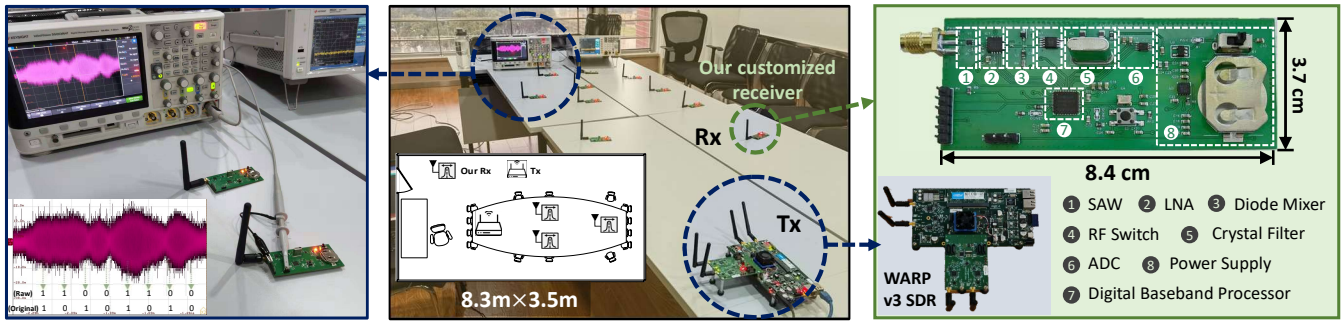


Figure 12: Prototype system and experiment setup. WARP broadcasts an OFDM+BPSK signal to our customized receivers. The DBP on each receiver processes the envelope waveform output from the crystal filter.

to filter out noise and other irrelevant signals. A low noise amplifier is to improve reception sensitivity. To realize down-conversion, we use the BAT15-03W RF Schottky diode as the first mixer, which is applied a bias current into the nonlinear interval. Demodulation is realized with an RF switch ADG902 [51] as the transistor mixer and a passive crystal filter ECS-10.7-7.5A [52]. To achieve the second-stage mixing, we generate the rectangular waves of arbitrary frequency with a DCO implemented in GOWIN GW1N-4B low-power FPGA [53]. The narrowband crystal filter not only takes out the selected subcarrier clean, but also transforms the signal's phase change into amplitude change. The amplitude variation is then extracted with a ADS7040 ADC [54]. The outcome undersampled digital signal is then decoded by a digital baseband processor (DBP), which is also implemented in the FPGA. More details are as follows.

Choice of Δf: We set the carrier signal frequency different Δf to be 10.7 MHz. This is close to the central frequency of the selected crystal filter f_0, which ensures that the minimum value of the signal frequency band is still greater than f_0. This is to reduce the interference of the frequency shift component in the second mixing process. In order to tune the signal to the LTE channel [1, 4, 5], the transmitter needs to accompany the OFDM signal to transmit a clean carrier below the channel frequency f_0.

SAW filter and LNA: In our prototype design, we set the OFDM signal's central frequency and bandwidth to be 2.412 GHz and 10 MHz, respectively. The TA2238A SAW filter is sufficient to filter out-of-band signals clean and minimize interference signals entering into the subsequent circuits. For the ultra-low-power low-noise amplifier, we use Nordic Semiconductor NRF21540 to obtain 13 dB RF gain, which can provide compensation for the path loss of the circuit, conversion loss of the mixer and the insertion loss of the filter. This makes the amplitude difference after the phase model conversion more obvious, which facilitates the final signal demodulation.

Diode mixer and transistor mixer: The conversion loss of the mixer mainly depends on the input signal strength, bias current and other factors [42]. For the chosen diode in our prototype, the conversion loss is minimized when the bias current is equal to 0.75 mA. For the transistor mixer, we use the ADG901 absorbing radio frequency switch, which can effectively avoid signal leakage. The signal isolation is 60 dB at least and the insertion loss is less than 0.4 dB.

Crystal filter: The crystal filter (ECS-10.7-7.5A) meets our design requirements, where the cutoff frequency is about 4 kHz and the stopband attenuation is more than 40 dB at 14 kHz. To obtain the desired performance, there is a need to perform impedance component matching, capacitance component matching, and inter-stage capacitance matching as described in Section 4.2.

ADC: We use a low-speed ADC ADS7040 with IQ sampling, which consumes only 44.5 μW at the sampling rate of 40$kSPS$, and the amplitude signal from the filter can be extracted and sent to DBP demodulation with very low power consumption.

DBP: DBP is responsible for generating square wave of subcarrier frequency, streaming it to the transistor mixer as the control signal. It is also used for demodulating the waveform data sampled by the low-speed ADC and decoding the data. The DBP is implemented using Verilog and deployed on the FPGA. The demodulation logic is illustrated in Fig. 9 and the DCO logic is shown in Figure 11. The receiver is allocated with a subcarrier index and this is mapped to a control word. That control word controls the DCO sigma logic to generate a square wave with the target subcarrier frequency for the second-stage mixing.

6 PERFORMANCE EVALUATION

This section evaluates performance of our prototype system. Experimental results are measured under the 0 dB LNA gain by default. The transmitter sends OFDM signal and the company carrier in Wi-Fi CH1 band, with transmission power 22 dBm+. We set the center frequency of the OFDM symbol and that of the company carrier Δf = 10.7 MHz away from each other. There are 12 subcarriers concurrently transmitted with subcarrier spacing is 10 kHz. On the receiver side, the bias current of the diode for passive down conversion is set to be 0.75mA for most conversion gain as used in [42]. The evaluation procedure does not raise any ethical issues.

6.1 Subcarrier Separation

We first examine the robustness of the proposed two-stage mixing scheme. The output of the filtering procedure depends on the accuracy of the oscillator involved. Frequency inconsistency between the local oscillator and that used in the transmitter can degrade the receiver sensitivity.

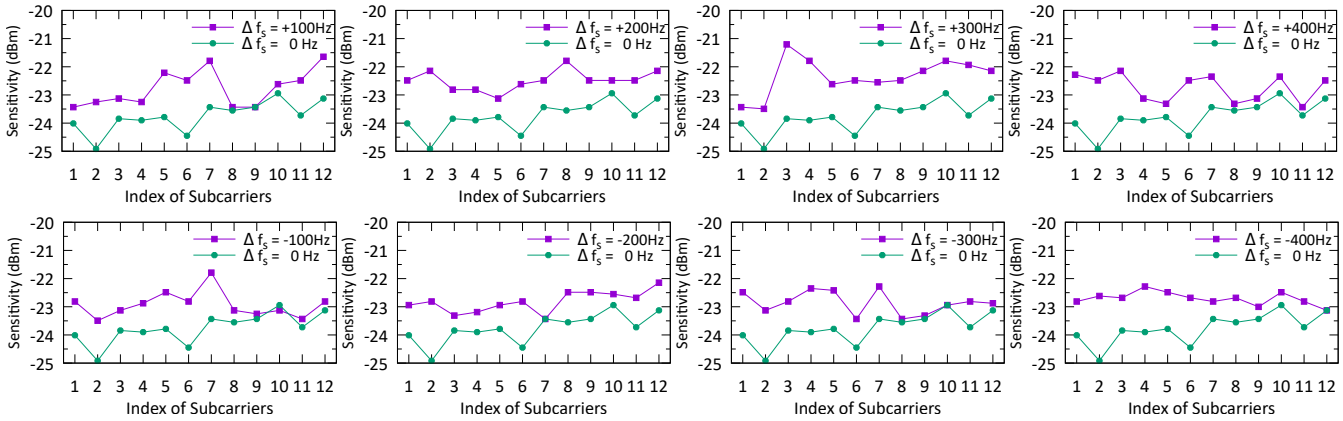


Figure 13: Impacts of frequency offset on RX sensitivity in terms of subcarriers.

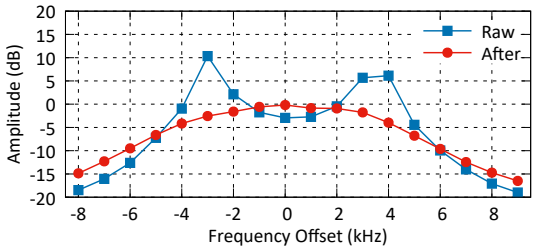


Figure 14: Magnitude response of crystal filter before and after impedance matching. Zero frequency offset corresponds to center frequency f_c = 10.7 MHz.

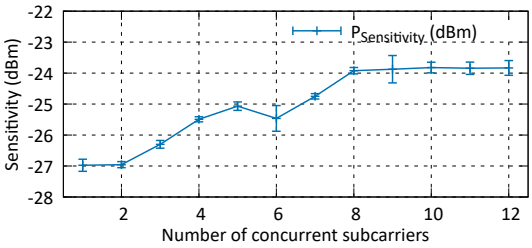


Figure 15: Impacts of ICI on RX sensitivity.

In the first-stage mixing, since both the received OFDM symbol and the company pure carrier are generated by the transmitter thus share the same local oscillator, there is no carrier frequency offset (CFO). However, the receiver circuit needs to shift the frequency of the received signal in the second-stage mixing, which involves the local oscillator that may have different properties from the one used in the transmitter. The crystal unit's stability is typically $\pm 10ppm$, and the maximum signal frequency generated in the second-stage mixing is 120 kHz, thus the maximum TX-RX frequency offset is around 1.2 Hz.

We investigate robustness of the prototype system considering $-400Hz \sim +400Hz$ TX-RX frequency offset. This is for sufficient safety margin, because the OFDM symbol may contain more subcarriers. In such frequency offset setting, the sensitivity of the receiver for subcarriers with various frequencies are shown in Fig. 13. The offset is intentionally added at the transmitter in experiments. The baseline is the sensitivity of all subcarriers without adding extra frequency offsets. We can see from Fig. 13 that the receiver sensitivity loss is within 4 dB, and most sensitivity loss is within 2 dB. The robustness of the proposed two-stage mixing procedure is verified.

6.2 Band Pass Filtering

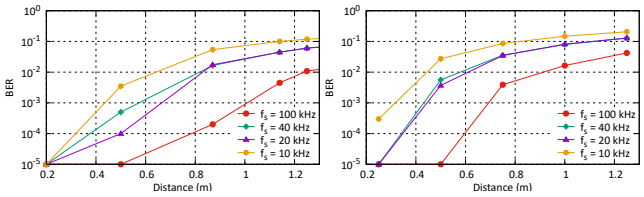
We here first investigate the magnitude response of the crystal filter and then show the filter's suppression on inter subcarrier interference.

The magnitude response $|H(f)|$ is shown in Fig. 14. The x-axis is the frequency deviation $f - f_c$, where f_c = 10.7 MHz is the center frequency of the filter. The blue curve is the $|H(f)|$ of an MCF and the red curve is the $|H(f)|$ of the MCF after impedance matching. We can see that after impedance matching, the passband response is more smooth, thus preventing nonlinear distortions to the subcarrier waveform. To take out a 10 kHz subcarrier, the crystal filter has an attenuation of over $20dB$ for adjacent subcarriers.

To further investigate the inter-subcarrier interference caused by non-ideal filtering, we increase the number of subcarriers in the OFDM symbol from 1 to 12, and record the receiver's sensitivity changes in Fig. 15. This is realized by adding zeros to unused subcarrier ports of the IFFT module in the OFDM transmitter. We can see that the sensitivity reaches $-27dBm$ when there is only one subcarrier. After adding more subcarriers, the sensitivity declines due to inter-subcarrier interference. After there are over 8 subcarriers, the sensitivity becomes unaffected. This is because those added subcarriers are too 'far' away from the filter passband and are completely eliminated. Such results indicate that our design can be extended to more subcarriers due to enough attenuation over those far-away subcarriers and the corresponding interference can be neglected.

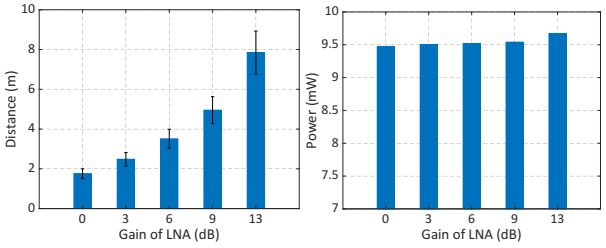
6.3 LOS and NLOS Performance

We test the LOS and NLOS performance of our receivers under different ADC sampling rates as shown in Fig. 16. The LNA is bypassed in this test corresponding to the 0 dB gain setting. BERs under different distances are measured. Our experiments are conducted in a meeting room as shown in Fig. 12. For the BER readings less than 10^{-5}, we set the corresponding values in the figure to be 10^{-5} to avoid meaningless points in the log-scale plotting. In



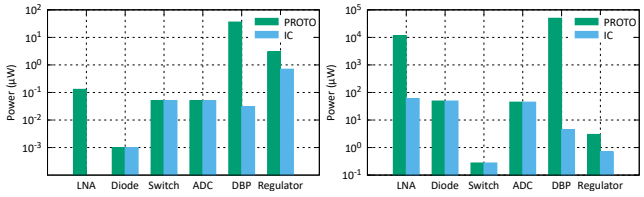
(a) LOS (b) NLOS

Figure 16: BER with distance.



(a) Distance vs. LNA Gain (b) LNA Power vs. LNA Gain

Figure 17: Distance and LNA power consumption with different LNA gains.



(a) Sleep Mode (b) Active Mode

Figure 18: The power consumption of our prototype and IC simulation results.

NLOS setup, we place a paper box filled with PCB boards between the TX and RXs. Results show that the communication distance in NLOS setup is less than around $1m$ for the $BER = 0.2$ point. ADC sampling frequency also affects the BER. We apply the same signal processing workflow under different sampling rates. We can see that the 10 kHz sampling rate has the worst performance, and 20 kHz achieves a good trade-off in performance and power consumption because the ADC power increases linearly with the ADC sampling frequency.

6.4 Range Improvement

Although our receiver circuit seems to have limited operation distance in Fig. 16, note that the result is measured under $0dB$ LNA gain (bypassed). If we allow more power consumption, the sensitivity can be improved so that the distance can be enhanced. We test the operating distance under different power amplification gains as shown in Fig. 17(a). The distance is tested under the LOS scenario, and the distance increases to $7.8m$ under 13 dB LNA gain. The IC power consumption of adding LNA for range improvement is to be presented below. In our prototype, the LNA power consumption under various gains is shown in Fig. 17(b).

6.5 Power Consumption

Prototype power consumption. The prototype power consumption comes from the LNA, diode mixer, transistor mixer, ADC, regulator and the FPGA, and the corresponding power consumption is illustrated in Fig. 18. The total power consumption in the active mode is 61.3 mW. We can see that the LNA and the FPGA consumes 99.87% of the total power consumption. In the sleeping mode with LNA shut down and FPGA standby, the power consumption can be reduced to 39.23 µW. The average power consumption under 1% duty cycling is 652 µW.

IC power consumption. The power consumption of LNA and the DBP can be significantly reduced with IC design. The LNA power can be reduced to 60 µW [55]. For the DBP, we use Synopsys DC for power simulation of the RTL design verified in FPGA based on 1.1V SMIC 40nm LP process. The power consumption of DBP is reduced to 4.5 µW. The total power consumption is 137 µW, mainly limited by the LNA, diode, and ADC. We note that this power consumption can be reduced to < 1 µW after 1% duty cycling. We note that 3GPP estimates that the NB-IoT receiving power consumption is around $3 \times 10^4 \mu A \times 3.3\,V = 99$ mW [56]; however, comprehensive measurements on commercial NB-IoT devices show that the actual power consumption is about 213 mW [18]. In this sense, the proposed design saves 130× power compared with the traditional design adopted by the commercial NB-IoT device. Here we assume that 12 receivers work together to demodulate the complete OFDM signal to give a fair comparison. If each receiver only uses one subcarrier, then the proposed design's power saving could be up to 1500×.

6.6 End-to-end Data Communication

To investigate the performance of the system when an application-level data stream is sent, we let the transmitter send a bitstream with application data to the receiver circuits. The data is the temperature value in 16 bits. It mimics real data collected from the HDC2080 temperature sensor [57]. Before transmission, the raw stream is first appended with a cyclic redundancy check (CRC) code with 4 bits long at the end; and the used CRC-4 polynomial is $z^4 + z^3 + z^2 + z + 1$. After that, the bistream is added with a preamble of 8 bits long at the beginning. As a result, the final frame length is 28 bits. We calculate the packet loss rate based on the counts of missing detection of the preamble; then the packet error rate is obtained based on the CRC check errors of the received frames. In the experiment, we let WARP v3 transmitter operate at 2.412 GHz and send frames repeatedly at a fixed time interval of 10 ms. In the low-power receiver circuit, we enable the LNA at 13 dB gain to provide the best range performance. The DBP sampling rate is set to 1 MHz and the parameter a of the mean filter is set to 200 (which corresponds to 0.2 ms) for overall performance under different settings. The final results are averaged from subcarriers 1-12. The spacing between two adjacent subcarriers is set to 20 kHz by configuring the DCO. Both the AFE output and the DBP output are monitored to locate the frame arrival and perform data decoding. The receiver is placed at various distances from 1 m to 7 m. The final performance of the packet loss rate and the packet error rate is shown in Figure 19.

7 DISCUSSIONS

■ **Limitations of the prototype.** The communication distance of our receiver can be further enhanced. In particular, we could use

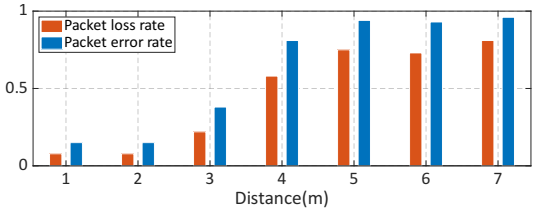


Figure 19: Packet loss rate and packet error rate of application-level data communication.

LNA as mentioned in Section 6.4, which makes the distance increase from 2.3 m to 7.8 m. Actually, we can spend more energy budget on amplification to improve range. Modern heterodyne receiver design such as [21] typically contains three amplification stages (RF, IF and baseband) for high sensitivity. In our design, we only employs an optional RF amplifier (LNA). Compared with the amplification of the digital receiver framework, our analog framework only consumes $1/N$ (N is the number of subcarriers in the OFDM symbol) power because only the filtered subcarrier experiences the amplification. Our design saves power by preventing the amplification of other users' signal.

Apart from active amplification, there are mainly three methods that can passively extend the communication distance without consuming more power. **a) Changing the frequency band.** Changing the frequency band to sub-GHz can increase the distance by reducing the path loss under the same distance. We could use back-of-the-envelope calculations to estimate the communication distance that could be possibly enhanced. Suppose that we add 56 dB IF amplifier as used in [42] and switch to the NB-IoT B20 band (800 MHz), then the distance can be increased to around 250 m with about 75.2 µW extra power consumption. The power saving is still 84 – 1000× compared with the commercial NB-IoT device. **b) Applying passive transformers.** Recent advances in nanowatt-level wakeup receiver use high-Q passive transformer to provide up to 20-25 dB passive gain after the antenna [58–61]. However, a drawback of this method is that the size of a high-gain transformer is in centimeter-level size, which will significantly increase the total size of the receiver circuit. Moreover, a high-gain transformer is difficult to fabricate for a frequency band in GHz level. **c) Replacing the SAW filter.** Although the SAW filter can effectively remove unnecessary out-of-band signals and thereby reduce the amplification power of that part, it introduces in-band attenuation of up to 3.2 dB [62] over the productive signal. It can be translated to around 3 meters of distance loss under the highest LNA gain. Replacing the SAW filter with low-temperature co-fired ceramics (LTCC) filters like TDK DEA162450BT can reduce insertion loss to 1.3 dB [63], which can be translated to around 1.5 meters enhancement in communication distance. However, it is at the cost of worse out-of-band attenuation performance (around 40 dB at 100 MHz away from the center frequency) compared to the SAW filter (around 10 dB at 100 MHz away from center frequency).

For the concurrency, in our prototype, 12 devices concurrently receive the signal with different payloads. The concurrency can be extended without degrading the receiver sensitivity. This is because further inter-subcarrier interference caused by the non-ideal filtering can be neglected when the subcarrier number exceeds 8 as verified in Section 6.2. However, the cost brought by subcarrier increment has two aspects: 1) The DBP needs to provide a higher frequency square wave for the second mixing, which increases power. Note that the maximum mixing frequency is $N \times \Delta BW = BW$. Since in LTE and Wi-Fi, a widely used BW is 20 MHz with 1200 concurrent subcarriers, the final power increment can be estimated to be around 9.4 µW under 40nm IC process [64], which means only 6.8% of total power increment. 2) The transmitter requires higher total transmission power to maintain the allocated power of each subcarrier.

As mentioned in Section 4.3, our proposed non-coherent detection scheme suits BPSK best. For higher-order PSK modulation or QAM, the transition of constellation points can be ambiguous in envelope changes thus the system performance could degrade. However, the data rate requirement for the IoT application is low, for example, the NB-IoT system only supports BPSK and QPSK. For QPSK, those symbol transition patterns still can be identified in our scheme if a higher sampling frequency ADC is applied.

■ **Multiple subcarriers in a single RX.** One advantage of OFDM modulation is the ability to tolerant multi-path effects, since the data stream is interleaved on multiple subcarriers. However, each receiver only uses a single subcarrier in our system, which may suffer from frequency-selective fading. To realize multi-subcarrier demodulation based on our framework, we can combine m single-subcarrier receivers together to make an enhanced receiver. Such receiver consumes m times the power consumption compared with the one use only single tone.

■ **Requiring modifications to the transmitter.** Although our OFDMA transmitter design needs modifications to existing OFDM transmitters like NB-IoT or Wi-Fi as introduced in Section 4.4, we do not incur new complicated modules. Instead, the modifications are mainly about bypassing some steps like adding CP and inserting pilot tones. Therefore, it is totally possible to implement such a design in an embedded SDR or a cellular system with modest modifications. Moreover, due to the adoption of reprogrammable BBU in LTE base stations, the transmitter design can be realized via firmware updates.

■ **Potential applications in NB-IoT.** The proposed design could be a reference for NB-IoT to further improve power efficiency. In this vein, our receiver design needs two main adaptations: 1) Wider bandwidth of the crystal filter circuit. The prototype receiver currently has a bandwidth of 10 kHz, but the NB-IoT standard needs 12 kHz. This can be resolved by cascading several MCFs with different poles to produce wider bandwidth. 2) We need to change the LNA to support NB-IoT bands. The design of TX also needs modifications, as mentioned in Section 4.4. However, changes are needed only in the digital domain, no need to touch the AFE. Such changes could be applied to NB-IoT at low cost, considering that the cellular network is evolving towards a cloud based radio access networking (C-RAN) architecture, where baseband units of base stations are deployed in the cloud in a centralized manner [65].

■ **Ultra-low-power OFDMA uplink.** Recent advances in backscatter communication already enable ultra-low-power OFDMA uplink [66, 67]. OFDMA backscatter [66] is implemented in the 802.11g framework while Digiscatter [67] is a customized OFDMA system that supports up to 1024 subcarriers with 19.5 kHz frequency spacing. OFDMA backscatter tags passively reflect the pure-tone signal sent by the transmitter (helper device) with frequency shifts.

Different frequency shifts are physically mapped to different subcarriers, which allow hundreds of tags to realize OFDMA uplink at the power consumption of 18 − 60 µW. It can be speculated that the design can be transferred to other OFDMA systems like NB-IoT. The design of the OFDMA backscatter uplink is beyond the scope of this paper, however, our design can be integrated with the OFDMA backscatter circuit because both the circuits are low-power at the μW level. Then it is possible to realize both ultra-low-power uplink and downlink simultaneously. Its total power consumption is expected to be less than 197 µW.

8 RELATED WORK

Cellular IoT standards. OFDMA downlink is based on the orthogonal frequency division multiplexing (OFDM) modulation scheme, which is the cornerstone physical layer technique for LTE, 5G and 5G beyond by the 3rd generation partnership project (3GPP). Considering the particular demands of increasing IoT applications, 3GPP develops several new technologies that are backward compatible to existing cellular networks [2, 7], including LTE-M, NB-IoT and extended coverage GSM IoT (EC-GSM-IoT). The former two fully reuse the LTE architecture with OFDMA downlink, and the last one is based on legacy GPRS/EGPRS systems. The duty-cycling schemes for LTE-M and NB-IoT such as DRX and PSM are the same; the difference is that LTE-M provides higher data rate with higher modulation order [25]. 3GPP initiates the cellular IoT standardization from Release 13 [68–71], and has developed a long-term evolution plan, where the OFDMA downlink design is to be maintained and further enhanced [8, 21, 23–26].

Wi-Fi power saving techniques. OFDM is also adopted in Wi-Fi standards 802.11a/g/n/ac/ax [10–12], and IEEE makes a series of efforts to reduce power consumption in WLAN, such as WLAN PSM [10, 34–36], automatic power save delivery (APSD) [72], power save multi-poll (PSMP) [73], transmission opportunity power save mode (TXOP PSM) [74], TWT [11, 13–17]. The 11ax standard utilizes OFDMA in both downlink and uplink to provide stable and high-bandwidth wireless transmission in high-density WLANs, while achieving reduction of energy consumption with various schemes, including cascade indication [11–13, 16, 17, 75], TXOP PSM, intra-PPDU power save [11, 13, 16, 17, 75], and operation mode indication (OMI) [11, 13, 76]. The essence of all the work mentioned above is to prolong the device's sleeping time. T-Fi offloads power burden from end device to Wi-Fi AP based on asymmetric clock rates [77]. Its key idea is to reduce the uplink transmission power of the IoT device yet increase the clock rate of the receiver at AP. OFDMA Wi-Fi backscatter presents a novel OFDMA uplink design which significantly reduces end device's transmission power with backscatter [66]. However, backscatter communication does not save receiver's power. Some works perform down-clocking to reduce downlink RX power consumption [78–81] either in idle listening or data receiving. However, these works cannot support OFDMA because downclocking would cause aliasing of subcarriers which destroy the orthogonality according to the Nyquist's sampling theorem.

Distributed OFDM. SNOW is a kind of cellular-like sensor network working on the TV white space, which presents the Distributed OFDM (D-OFDM) design for both uplink and downlink [82, 83]. D-OFDM is essentially a simplified OFDMA scheme, where the strict transceiver synchronization is relaxed. For the downlink, the base station periodically broadcast the OFDM frame, which encodes data destined to different end nodes with different subcarriers. The end nodes still adopt the all-digital FFT based demodulation scheme, and the power saving scheme is also based on duty cycling. SNOW nodes present less than $60mW$ power consumption, which is obtained by estimating with the CC1070 RF module's energy model.

Analog method in downlink design. Saiyan is a low-power demodulation design for downlink LoRa backscatter systems, where the key technique is to transform the frequency-modulated chirp signal into amplitude-modulated signal using the surface acoustic wave (SAW) filter [43, 84–86]. Saiyan provides no support for OFDMA downlink or concurrency with the fixed circuit design that is non-configurable. MIXIQ is an ultra-low power Wi-Fi receiver, which replaces regular down converter with the diode [42, 43, 87]. The demodulation process after down conversion is still realized in the digital domain.

Ultra-low power wakeup receivers. The main difference between WuRX and normal receivers is that WuRX cannot demodulate an arbitrary protocol-compatible frame but can only detect the arrival of a certain RF pattern. It usually works as the pre-stage of a normal receiver for power saving. Recent advances include nanowatt wakeup receiver (WuRX) designs [59–61, 88, 89] and protocol-compatible WuRX designs based on back-channel modulation [58, 90, 91]. The key feature of WuRX is similar to that of this work: turning power-hungry components into passive and analog. However, WuRX's structure is extremely simple because it is designed to detect RF patterns and cannot demodulate packet data. A RF pattern is fixed in its bitstream and can be correlated by the WuRX, which wakes up the following circuits. For the same reason, WuRXs cannot realize the OFDMA downlink. In contrast, our design is not constrained to pattern detection but extended to productive data reception and can support multiple users' access by realizing OFDMA.

9 CONCLUSIONS AND FUTURE WORK

OFDMA downlink design as adopted by LTE, 5G and 802.11ax can effectively process many OFDM subcarriers in parallel, but suffers from high power consumption of the digital processing and corresponding ADC modules, which hinders its adoption in IoT applications with long battery life expectation of the receiver. Existing solutions to the issue are basically based on duty cycling, which makes the device inactive most of the time but still results in ≈100 mW power consumption. This is because the device's power demand when active is still high. In this paper, we present a OFDMA downlink demodulation technique that transfers the digital receiver framework to an analog framework. Our prototype system realizes 12 concurrent downlink receivers with 137 µW power consumption. It saves 130-1500 times power consumption compared to existing OFDMA receiver designs. Our evaluations show that our system can operate with a range of 7.8 meters. Future work is to enhance the sensitivity of the receiver and increases the downlink distance.

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